

# SIGNAL CONDITIONING

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## CONNECTING INPUTS TO LOGIC GATES

For a logic gate input to recognise the signal applied to it as logic 1 the voltage level of the signal should be as near as practically possible to the value of the supply voltage. Similarly for the signal to be recognised as logic 0 it should be as near as possible in value to 0 volts.

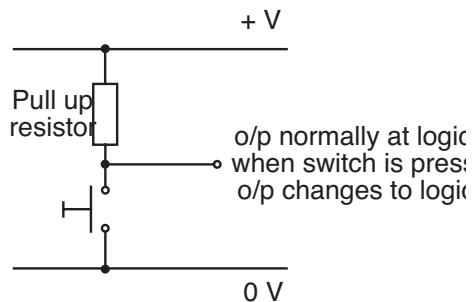
If the input signal changes from logic 0 to logic 1 or from logic 1 to logic 0 it should pass through the open band as rapidly as possible. This prevents the logic system behaving in an unpredictable way. See Study File 4 on logic gates for more information about logic levels.

We shall now consider how mechanical switches and light sensors are connected to the inputs of logic gates.

## CONNECTING MECHANICAL SWITCHES TO LOGIC SYSTEM

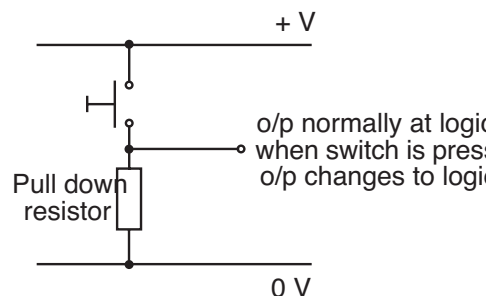
Consider the two circuits below:

(i)



The resistor is referred to as a pull up resistor because it pulls the output up to logic 1 when the switch is open. The value of a pull up resistor is not critical. A 10 k $\Omega$  resistor is usually used for TTL circuits and a value up to 100 k $\Omega$  for CMOS circuits.

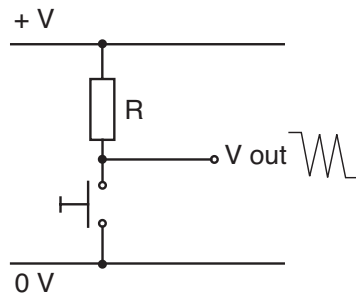
(ii)



In this case the resistor is referred to as a pull down resistor. The value of a pull down resistor should normally be less than or equal to 1 k $\Omega$  for TTL. For CMOS circuits resistors up to 100 k $\Omega$  may be used.

SWITCH BOUNCE

The contact blades of both mechanical and reed switches tend to 'bounce' when the switch is closed. This results in the voltage being switched on and off several times before the switch settles down.



When the switch is closed the output voltage  $V_{out}$  will change rapidly between 0V and 9V several times before settling down at 0V.

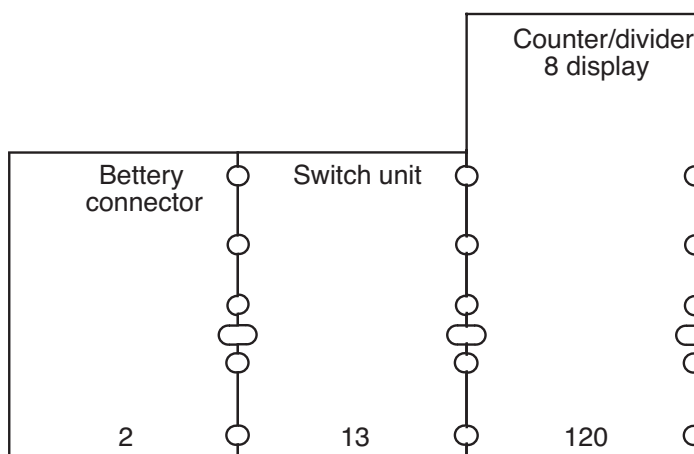
The effect is referred to as contact bounce or switch bounce.

Switch bounce would have little effect in a system consisting only of logic gates.

If a system contained an electronic counter then switch bounce would be highly undesirable. The counter will increment by several numbers each time the switch is pressed.

INVESTIGATION 1

Assemble the following counting system on Alpha or similar system boards.

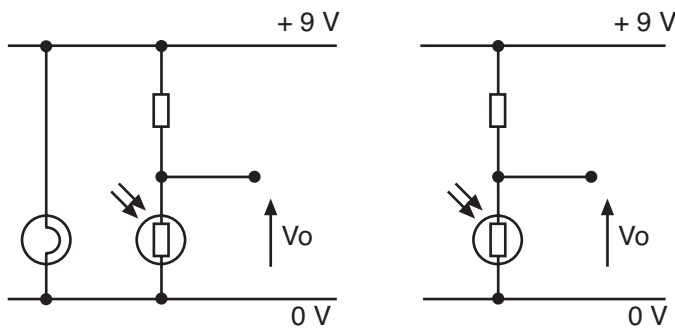


Press the switch slowly several times and observe the increase in the count registered on the display. Comment on the performance of the counting system.

Repeat the investigation with a different switch unit.

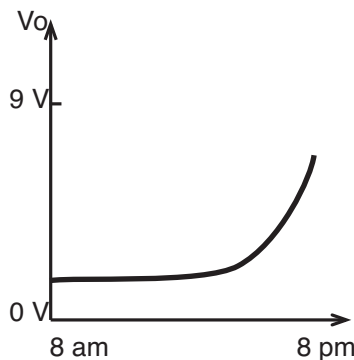
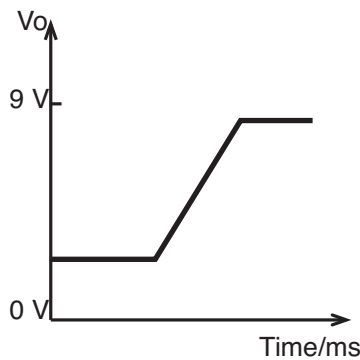
CONNECTING A LIGHT SENSOR TO A LOGIC SYSTEM

Consider the two light sensing units below.



The output  $V_o$  is low until the light beam between the bulb and the LDR is broken.  $V_o$  will take several milliseconds to go high as the LDR slowly responds to the change in light intensity as shown below.

In daylight the output  $V_o$  is low. As darkness starts to fall the light level gradually decreases and  $V_o$  will slowly increase. The change in  $V_o$  would possibly occur over several hours and  $V_o$  could be in the open logic band for a long period of time.



These slowly changing voltages would be of little or no use in controlling the input to a logic system which requires a signal that changes logic state in a few microseconds.

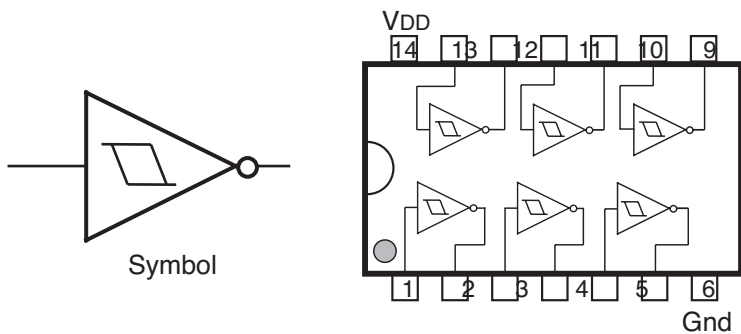
Slow changing signals from sensing circuits have to be processed or conditioned before they can be used with logic gates.

SCHMITT INVERTERS

Ordinary inverters have a single input voltage level which causes the output to change state. This voltage level is referred to as the threshold level.

A Schmitt inverter has the same truth table as an ordinary inverter but it has two switching thresholds rather than one. The switching threshold for a rising input voltage is higher than that for a falling input voltage. These thresholds have different values for different types of Schmitt inverter.

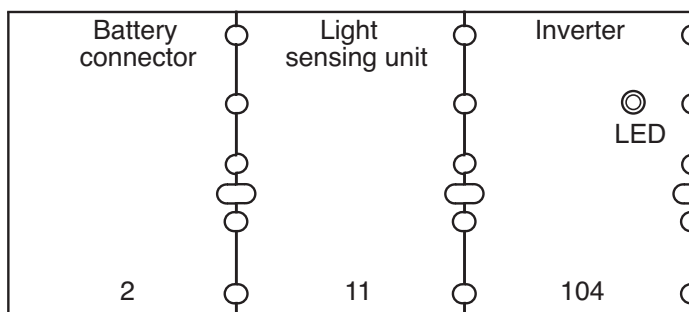
For example on a 9V supply a CMOS 40106 Schmitt inverter has an upper switching threshold of approximately 5.2v for rising input voltages and a lower switching threshold of 3.6v for falling input voltages.



Pin out diagram of a CMOS 40 Hex Schmitt inverter

INVESTIGATION 2

You will need fairly bright illumination to conduct this investigation. Assemble the following light sensing system.



Adjust the dial on the light sensing unit until the LED indicator on the inverter board is just off whilst the LDR is uncovered.

Slowly move your hand over the LDR and you should notice that more than one brightness of the LED can be obtained.

Try to explain why this is so.

### INVESTIGATION 3

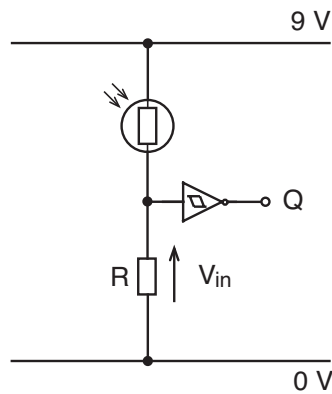
Connect a counter/display unit to the output of the system set up in investigation 2 and repeat the procedure. Comment on what you observe. Try to give a reason for what is happening.

### SIGNAL CONDITIONING

Schmitt inverter circuits are ideal for interfacing inputs to logic systems. They are particularly useful for eliminating unwanted noise, improving rise times and eliminating contact bounce.

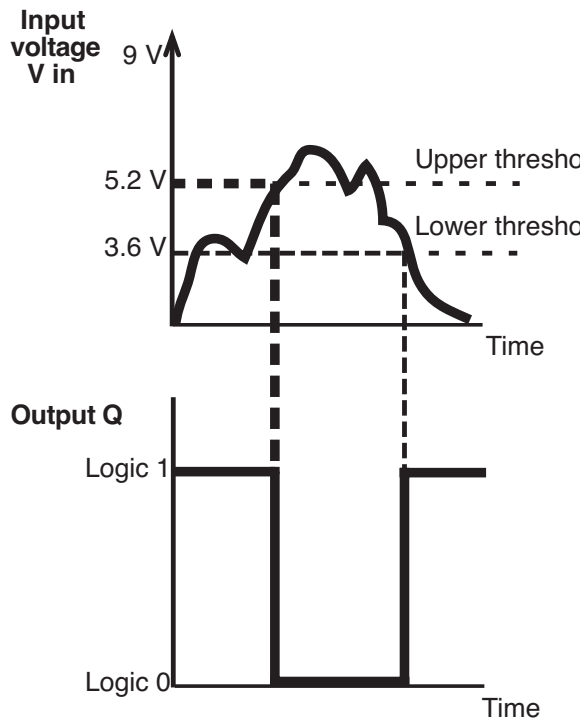
#### Example 1: Improving the rise time of an input sensing unit

Consider a signal from a light sensing unit being applied to a CMOS 40106 Schmitt inverter over a period of time.



In darkness the resistance of the LDR is very high, the input voltage  $V_{in}$  is nearly at 0V and the output is at logic 1.  $V_{in}$  increases as the light level gradually increases. The output,  $Q$ , remains at logic 1 until  $V_{in}$  increases to the upper switching threshold of the Schmitt inverter which is 5.2V. At this value of  $V_{in}$  the output instantly changes to logic 0 and remains there until  $V_{in}$  falls to 3.6V. At this lower switching threshold the output instantly changes to logic 1.

A typical graph showing how the output Q changes as  $V_{in}$  changes is given below.



You will notice there is a rapid transition between logic levels at the output Q as each of the input threshold voltages is reached. Minor fluctuations in input voltage are ignored.

The Schmitt inverter has conditioned the input signal to make it suitable for applying to the input of a logic system.

#### INVESTIGATION 4

Repeat investigations 2 and 3 replacing the inverter board with a Schmitt inverter board. Comment on any improvement that the Schmitt inverter has made on your system.

**Example 2: Switch Debouncing**

We have already investigated the arrangement shown in Fig.1 and discovered that the output voltage  $V_{out}$  changes several times before settling at 0V.

If a capacitor is connected across the switch as shown in Fig. 2 the capacitor will suppress but not completely eliminate the effect of the contact blades bouncing.

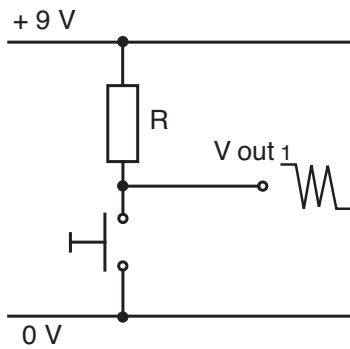


Fig. 1

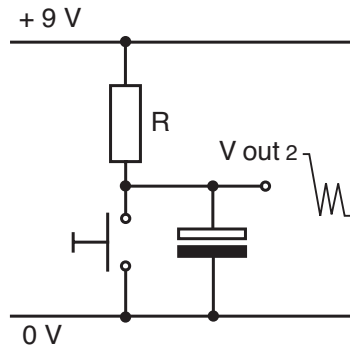


Fig. 2

Adding a Schmitt inverter as shown in Fig.3 will eliminate any effect of switch bounce at the output. The small fluctuations present in  $V_{out 2}$  are ignored by the Schmitt inverter since their value is much smaller than the upper threshold level of the Schmitt inverter.

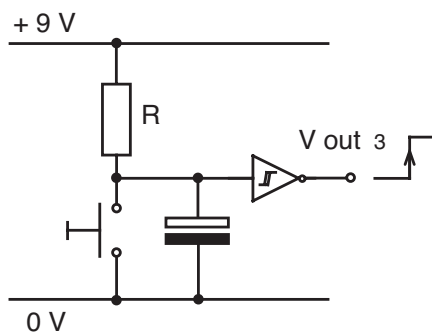
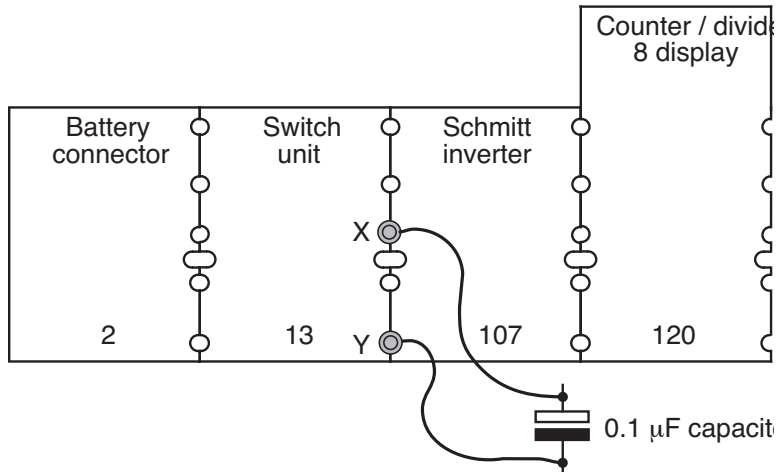


Fig. 3

INVESTIGATION 5

Assemble the counting system shown below.



Connect a 0.1μf capacitor between the points marked X and Y on the diagram. Compare the performance of this system with the results you obtained in investigation 1.

Repeat the investigation without the capacitor. You will probably get an unexpected result. Can you give a reason why?