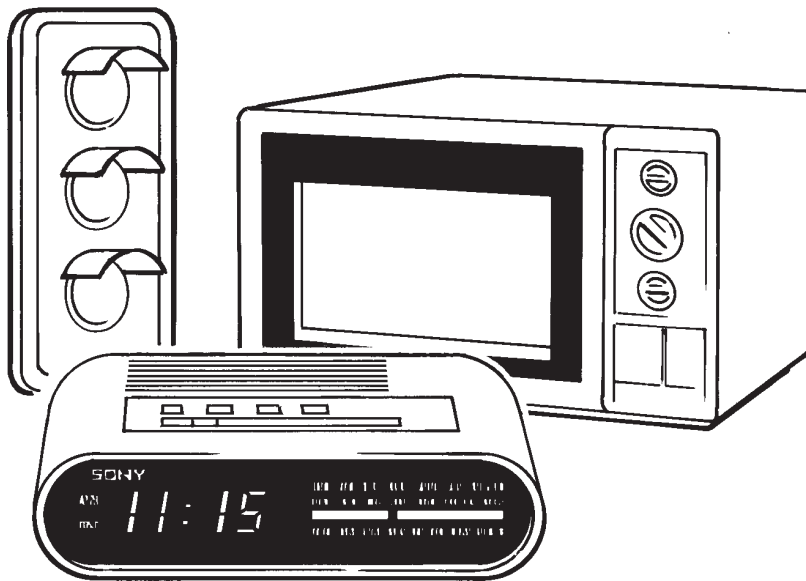


# DESIGNING AND MAKING A SEQUENTIAL ELECTRONIC TIMER

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Timers are very common in electronic systems. We can all think of situations in which a timer controls when something should happen or for how long it should happen. Most modern cookers and all microwave ovens have a timer to control how long food is cooked for.



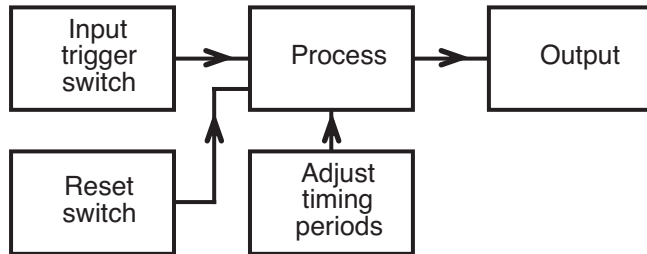
Pelican crossings have several timers which operate in sequence one after the other when triggered. Once the sequence is completed the systems return to its normal (or stable) state until it is triggered by another pedestrian. Such a system is referred to as a sequential electronic timing system.

## DESIGN BRIEF

Design and make a sequential electronic timing system that can operate up to four separate output devices in sequence one after the other. The length of time that each device is activated should be adjustable and independent of the other three outputs. The system should be capable of being triggered by either a momentary push of a switch or the opening of a switch. The timing sequence should be capable of being aborted any time by means of a reset switch.

### DESIGNING THE SYSTEM

The block diagram for the system is shown below.



The input block will provide one signal to trigger the sequence into action and another signal to allow the sequence to be reset.

The process block will consist of four timer sections connected in tandem or cascaded.

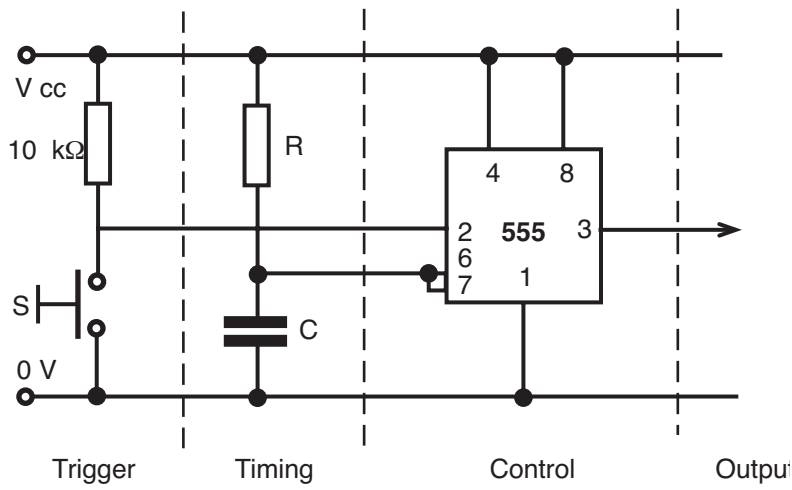
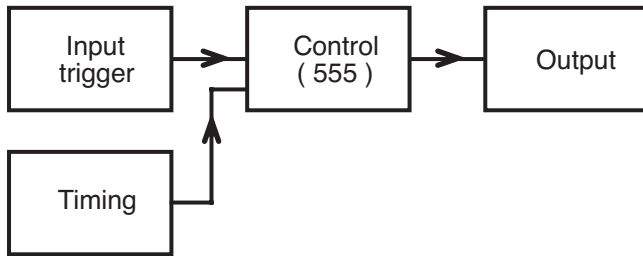
The output block will consist of a terminal strip to which a variety of output devices may be connected.

We shall consider the process block first since the triggering and reset design will depend on the properties of the process block. Similarly the range of outputs that can be activated will depend on the output current capability of the process block.

### PROCESS BLOCK

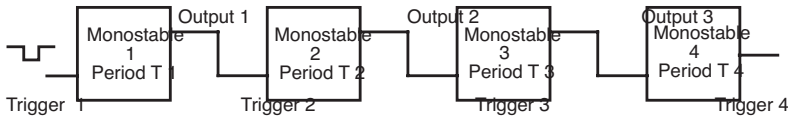
The most obvious choice for the Process Block is to use four 555 timer ICs configured as monostables. If you look at Study File 6 you will find that a 555 monostable requires a short pulse to trigger it.

A block diagram and a circuit diagram for a single 555 monostable are shown below.

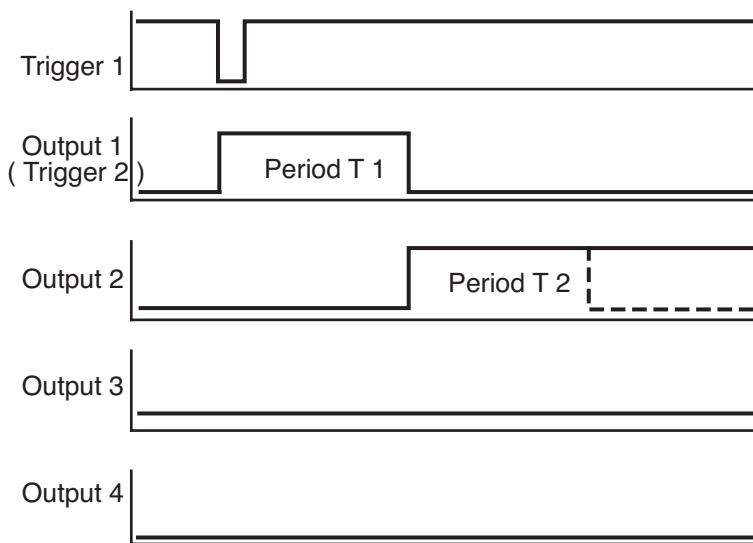


We can now extend this system to provide four timing periods.

Four cascaded 555 monostables having timing periods  $T_1$ ,  $T_2$ ,  $T_3$  and  $T_4$  respectively are shown below.



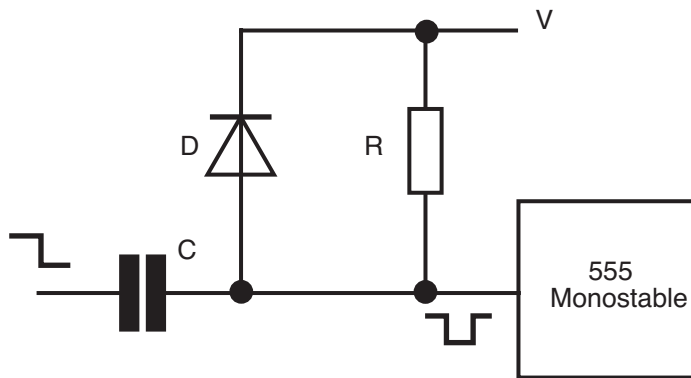
The timing diagram for this system is



When timing period  $T_1$  is completed the falling edge of the output waveform triggers output 2 high. Unfortunately output 2 will stay high indefinitely until monostable 1 is re-triggered, rather than going low at the end of period  $T_2$ .

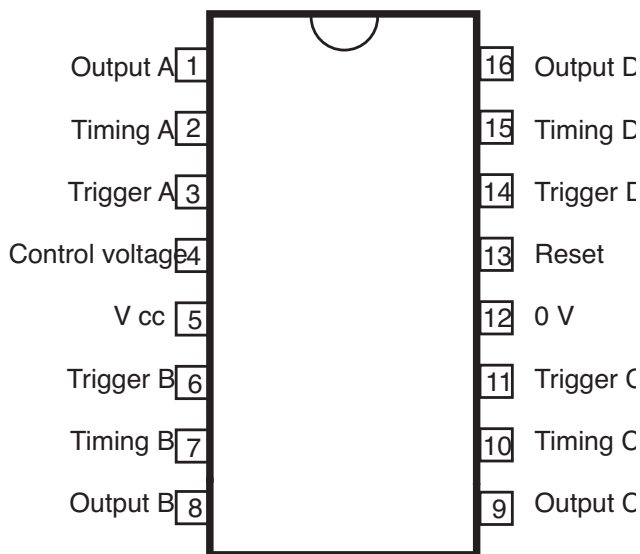
Outputs 3 and 4 will remain low.

555 monostables are said to be pulse triggered. To cascade monostables they need to be edge triggered. This problem can be overcome by using a differentiating network to provide a trigger input for each 555 timer as follows:

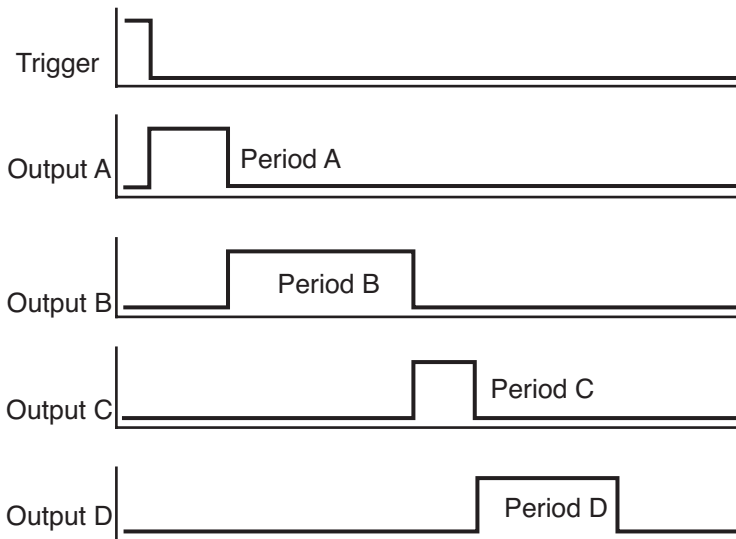
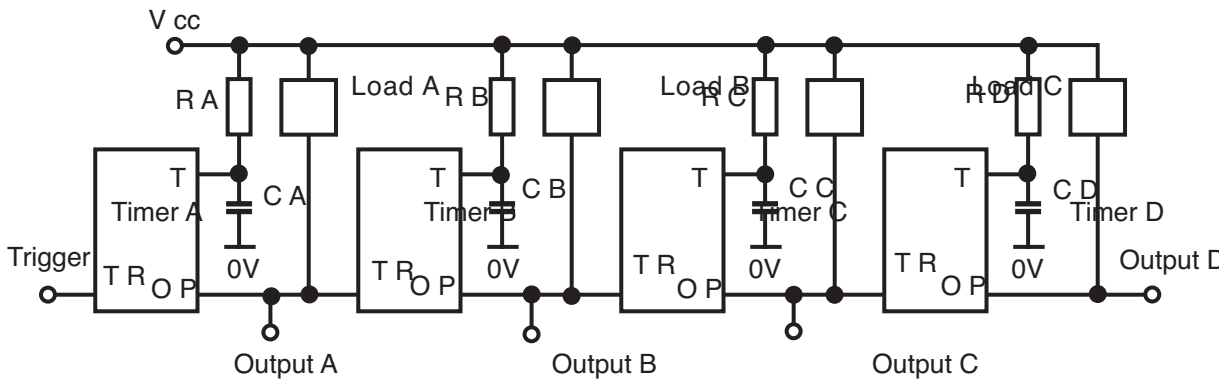


The disadvantage of cascading 555 timers for our design is that four ICs will be required and 12 additional components to provide edge triggering.

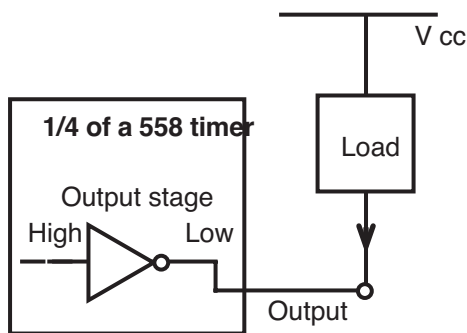
A more convenient option is to use a 558 Quad Timer which has the necessary internal circuitry to allow all four timers to be cascaded. The falling edge of the input signal applied to the first timer starts the sequence. A 558 Quad Timer is available in a 16 pin DIL package. The pin out diagram is shown below.



The following schematic and timing diagrams show how all four monostables can be cascaded to produce four timing periods which are independent of one another. Each monostable output goes high in sequence, one after the other.



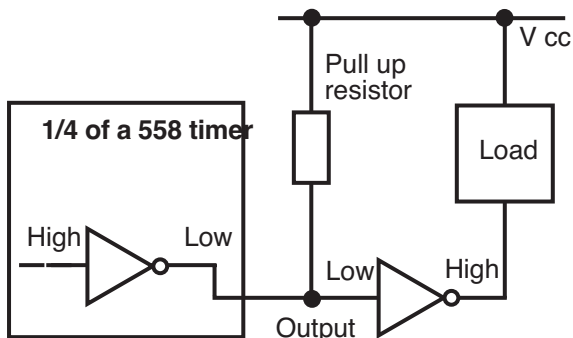
The output stage of each monostable timer is normally low in its quiescent (or stable) untriggered state. A diagram representing the signal levels is shown below.



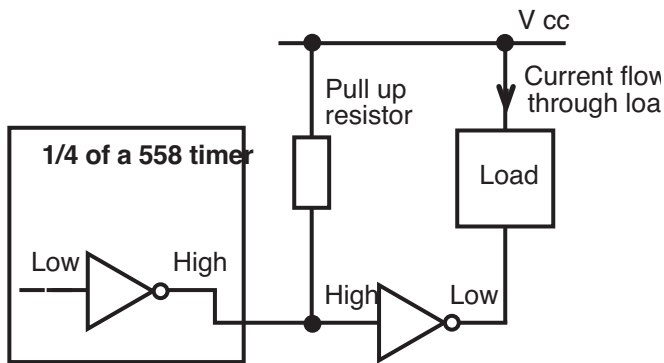
This means that the monostable output is sinking current and the output device is activated. When the input of a monostable is triggered its output goes high and the corresponding output device switches off for a predetermined time.

We require the opposite action, that is an output device being triggered on for a predetermined time.

A 558 timer output cannot source current so we have to invert the monostable output as follows.

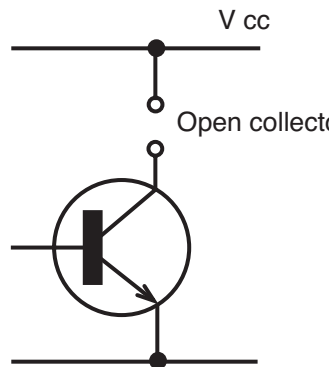


Signal levels during quiescent state



Signal levels during timing period

The pull resistor is necessary because the 558 timer is an open collector device. This means that the final transistor in each of the four output stages has its collector open circuited.

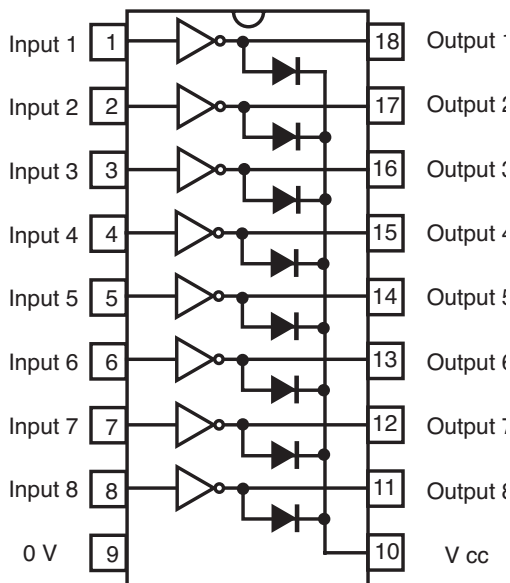


For an open collector device to function, the load or alternatively a pull up resistor has to be connected between Vcc and the open collector to complete the circuit.

You may at this stage wonder whether there is any advantage in using a 558 rather than four 555 timers since each 558 output requires a pull up resistor and an inverter. Actually there is still an advantage in using a 558 timer if we take the opportunity to increase the output current capability of our system by employing inverters that double up as drivers. One such device is the Darlington Driver which has a number of Darlington Pairs on a DIL package. See Study File 9 for more information about Darlington's.

**DARLINGTON DRIVER**

A schematic pin out diagram of a ULN 2807 Darlington Driver IC is shown below.



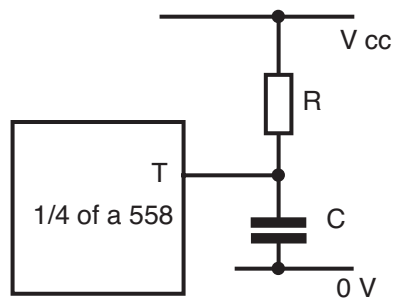
Each of the eight Darlington has an output current capability of 500mA. If necessary, pairs of Darlington may be connected in parallel to increase the output current capability to 1 amp. Each Darlington has a built in input protection resistor and an output protection diode to prevent inductive loads such as motors or relays damaging the IC. If a particular Darlington input is taken high, the corresponding output goes low, activating an output device connected between the positive supply and the output.

THE TIMING PERIOD

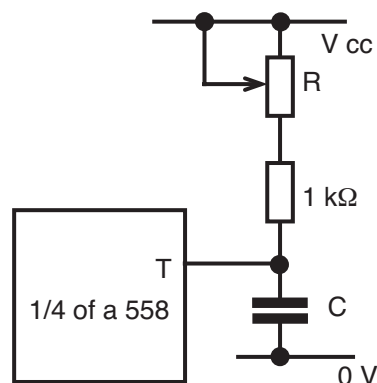
The timing period for which each monostable output is high is given by the formula

$$T = R \times C$$

when R is in ohm, C is in Farads and T is in seconds.



If a variable resistor is used for R then the period T can be adjusted. To prevent excessive current flowing into the 558 when R is adjusted to a small value of resistance, a 1 kΩ current limiting resistor is placed in series with R.

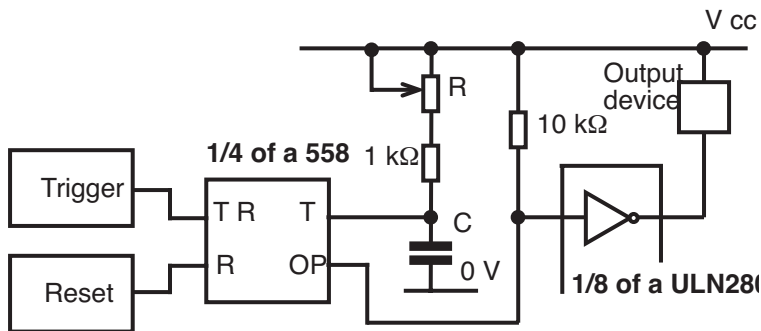


Study File 6 considers the timing period of a monostable in more detail.

Two values of capacitor and two values of variable resistor (in series with a 1kΩ protection resistor) should be able to provide a wide range of timing periods as indicated in the following table.

Required timing period/variable resistor Capacitor		
0.1 to 10 seconds	100 kΩ	100 μF
10 to 100 seconds	1 MΩ	100 μF
100 to 1000 seconds	1 MΩ	1000 μF

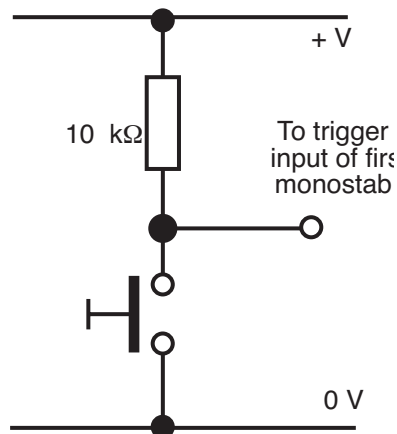
The block schematic diagram of one of the four sections of our system is as follows.



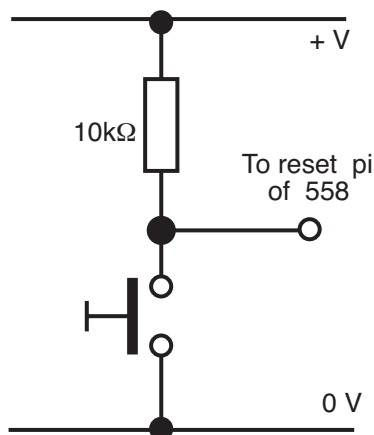
INPUT BLOCK

The first monostable in the chain of the four cascaded monostables has to be triggered by the falling edge of an externally applied pulse. The three other monostables are then automatically triggered in turn as long as the output of one monostable is directly connected to the trigger input of the next monostable in the chain.

A falling edge trigger pulse can quite easily be produced by a means of a push switch and a pull up resistor as shown below.

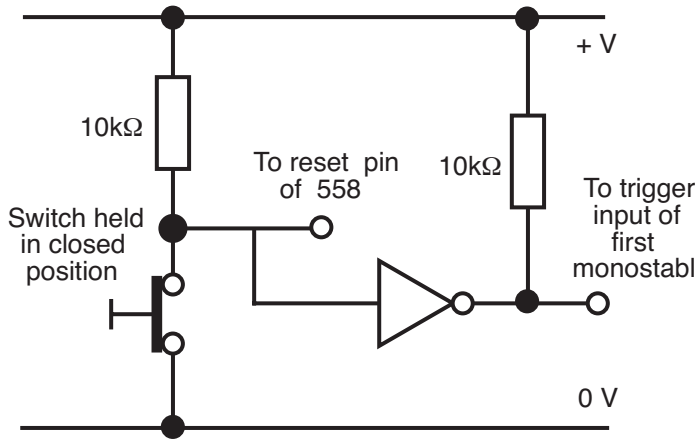


Similarly, all four monostables can be reset simultaneously to their normal quiescent state by the falling edge of a pulse applied to the reset input.



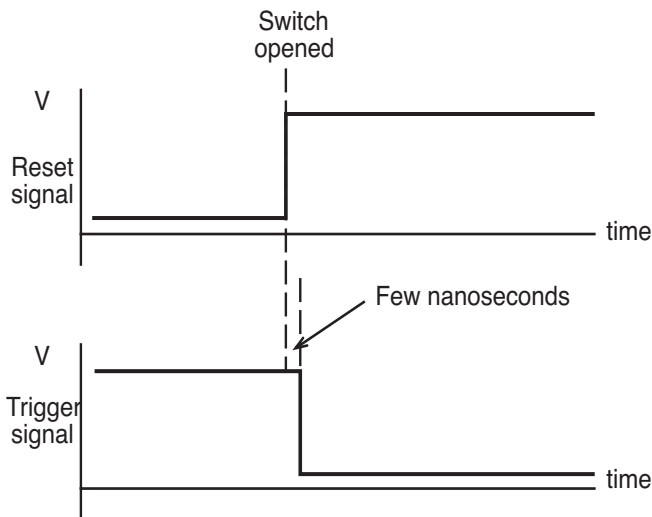
If the reset input (pin 13) is held low then all monostables are disabled.

The design brief also requires the system to be capable of being triggered by the opening of a switch. This can be achieved by combining the trigger and reset into a single switch as follows.



We can use one of the spare Darlington drivers as an inverter. You will notice that it requires a pull up resistor at the output.

The timing diagram for the combined reset and trigger is shown below.



When the switch is held closed by a door for example the system is disabled.

On opening the door the switch opens and the reset input goes high enabling the system. Fortunately, it takes a few nanoseconds for the inverter to respond to the signal changing at its input. Therefore the trigger input will not go low until the system has enabled, and the falling edge of the signal at the inverter output triggers the sequence into action.

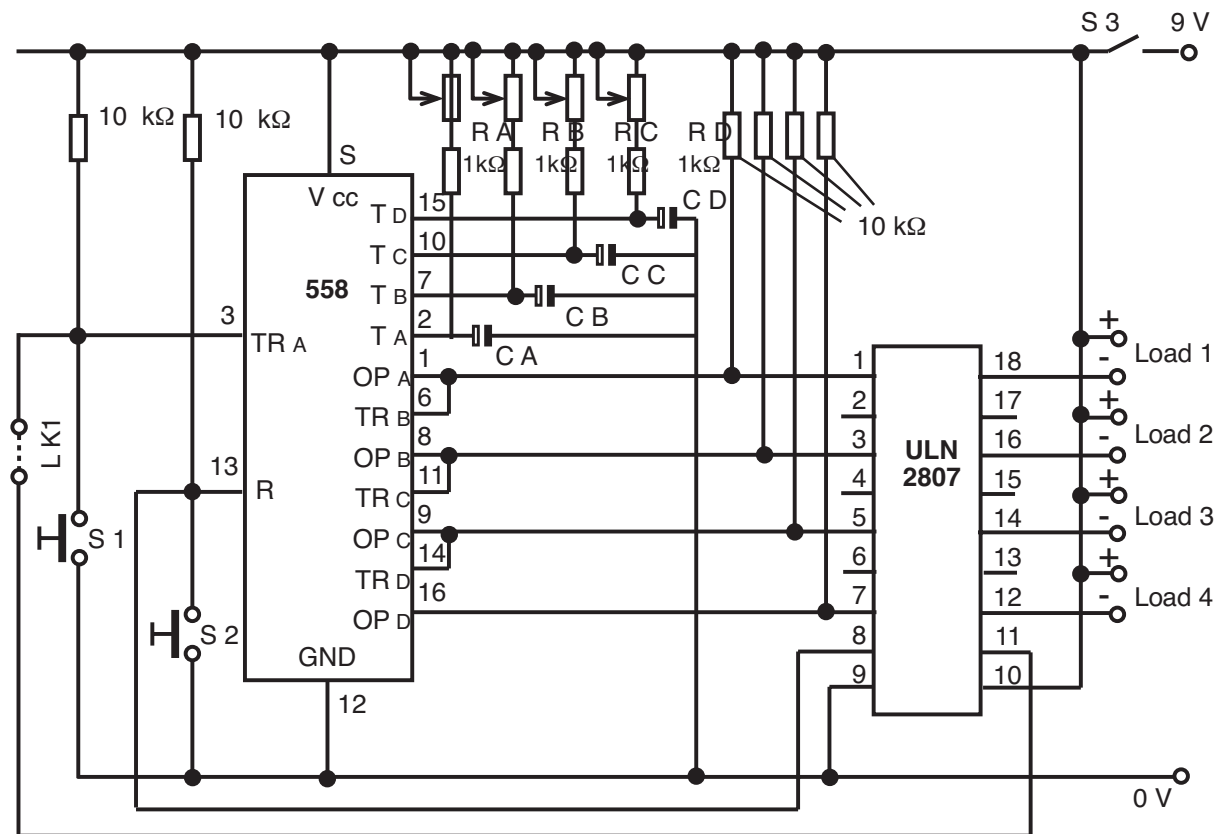
OUTPUT BLOCK

It is left to you to design the output block. The four outputs will be taken to a screw terminal block in which a whole variety of output devices may be connected.

Outputs such as LEDs will require a 680Ω current limiting resistor whilst outputs such as motors and solenoids may require two Darlington's to be paralleled up. These devices will require a power supply rather than batteries.

PUTTING IT ALL TOGETHER

The circuit diagram for the complete system is shown below.

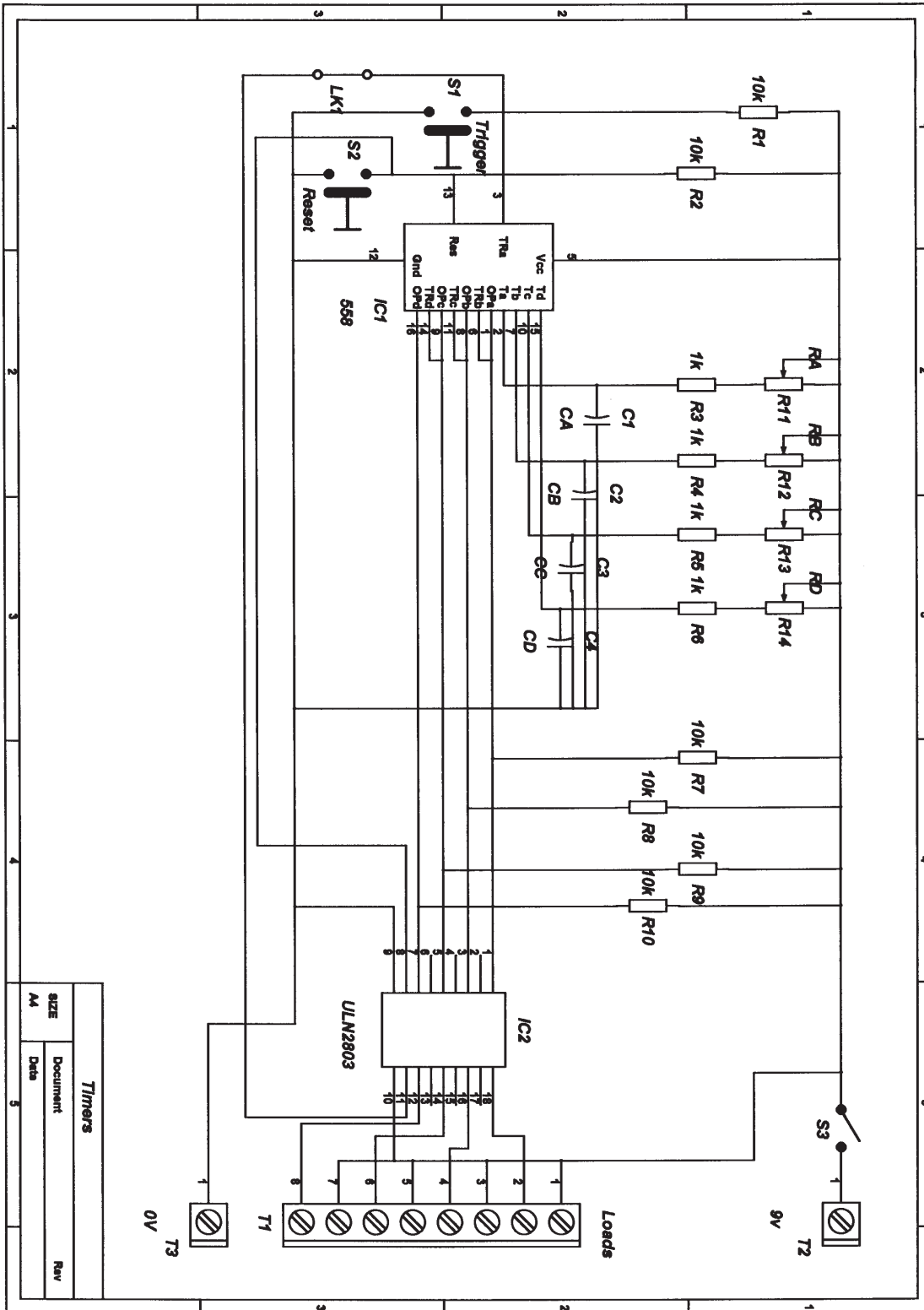


Note: Link LK1 is connected only if combined triggering and reset is to be used

You will need to make a printed circuit board (PCB) onto which to mount the components. To find out about this see Study File 8 (Making a PCB).

The following four drawings have been produced on a PCB design software package. A disk is also supplied containing a file which includes all four drawings. More information about the PCB design software is given in Study File 8.

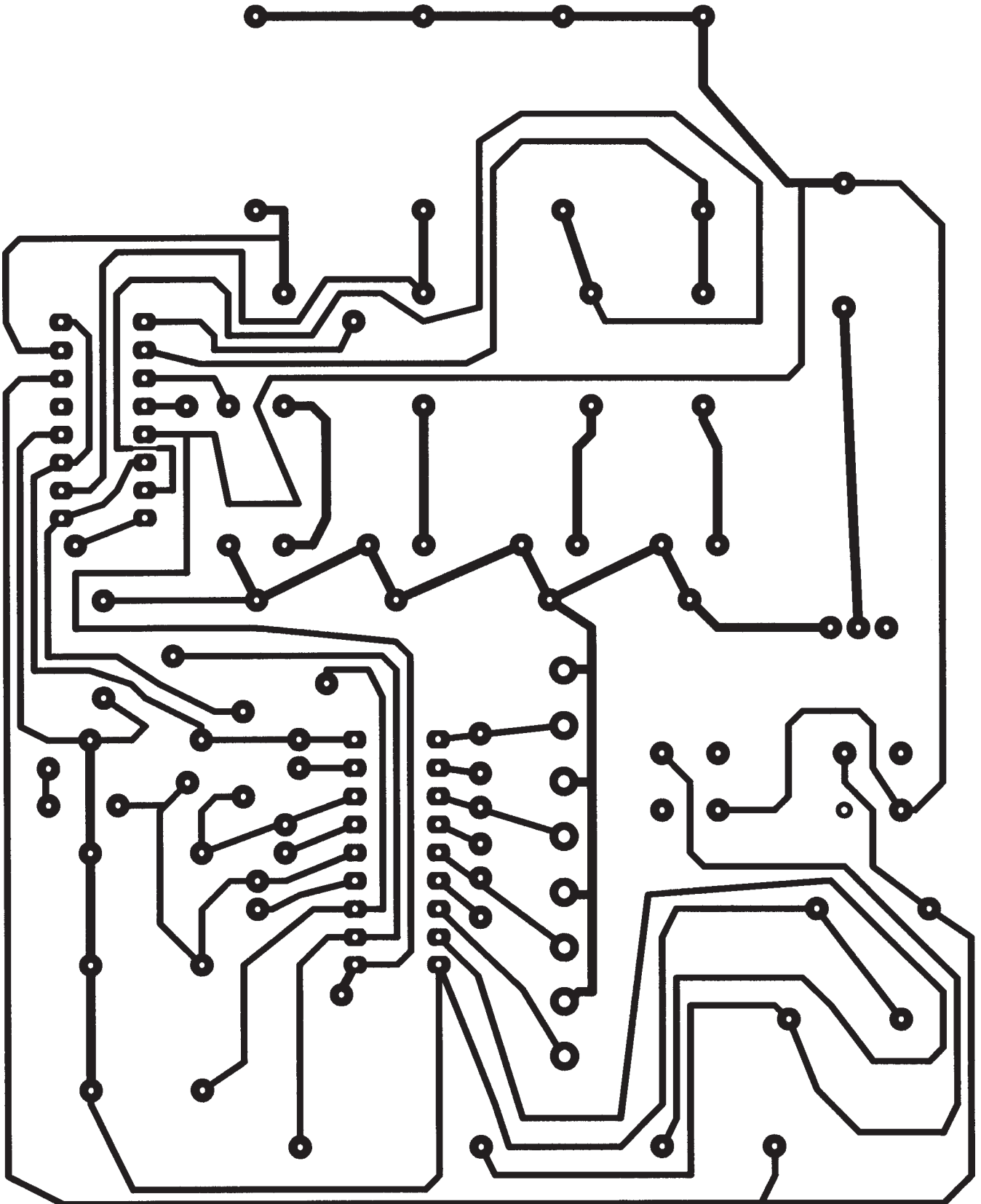
SCHEMATIC CIRCUIT DIAGRAM



This is the circuit diagram for the complete system redrawn by the design software. The software uses the diagram to create the other three diagrams.

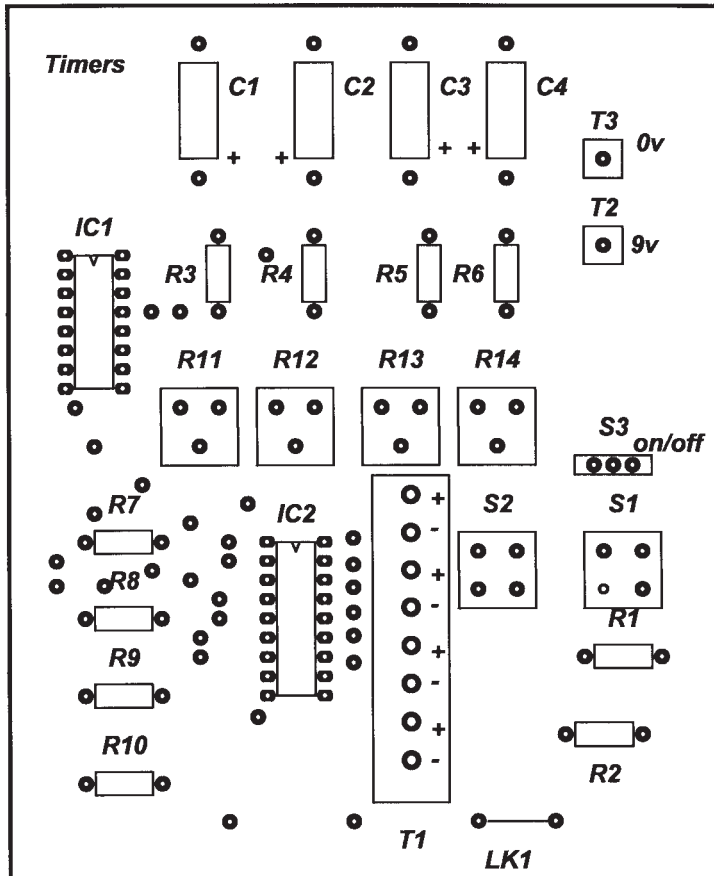
PCB LAYOUT DIAGRAM

This diagram is used to create the PCB mask on an acetate sheet as described in Study File 8. The diagram is supplied twice normal size so the photocopier should be set to 50% reduction when producing the mask.



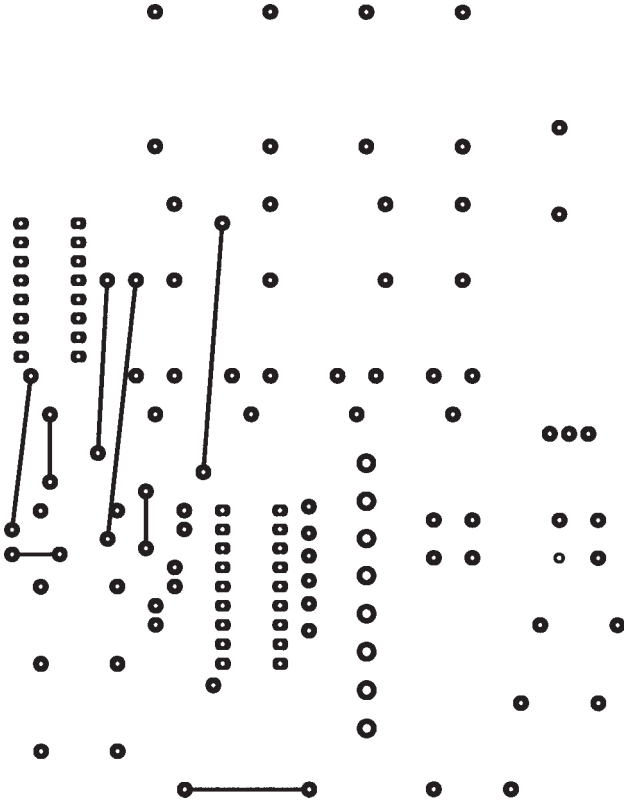
COMPONENT LAYOUT DIAGRAM

The diagram shows you where each of the components is to be mounted on the PCB.



WIRE LINK DIAGRAM

This diagram shows you where wire links have to be inserted.



It is advisable to mount all the IC socket holders first. Before mounting any other components you can check with a multimeter set to the 200Ω range to ensure that solder has not spilt on any tracks which pass between adjacent pins.

## TESTING

When you have built the circuit, you will need to test it to see if it works correctly.

Connect a load such as a buzzer or a 12V current limited LED to each of the outputs.

Adjust each of the four variable resistor controls to their mid position. The test you perform will depend on whether you have separate or combined trigger and reset.

Where separate triggering and reset is used link LK1 is left disconnected. Press S1 and each of the four output devices should be activated in turn for approximately the same length of time. Press S1 again and press S2 half way through the sequence to ensure you can reset the system.

Where combined triggering and reset is used link LK1 is connected and switch S1 is left out.

In this case hold S2 down and all outputs should be off. Releasing S1 should start the sequence and each of the four output devices will be activated in turn. If S2 is held down at any time the sequence should stop and the system will reset.

In each of the two situations check that the on period of each output device can be adjusted without affecting the other outputs.

If the circuit does not work, follow the simple Fault Finding procedure below:

1. Check that no tracks or pads are bridged or broken. Repair if necessary (see Study File 8).
2. Check that all solder joints are good.
3. Check that all components are mounted correctly. Pay particular attention to the ICs. It is quite easy to plug them in the wrong way around.
4. If all this fails try changing the ICs.

### EVALUATING THE TIMER SYSTEM

There are a number of things you need to consider when evaluating the system.

1. How well does it work?
  - Is the range of periods available for each output adequate?
  - Can the timing period of each output be adjusted accurately?
2. Will it work in the situation for which it was designed?
  - Can the timing periods be calibrated?
  - Can different types of output be easily connected?
3. Is the system robust enough?
  - Have you mounted the circuit in a project box?
  - Are the controls and output terminals easily accessible?